# Broadband Highly Integrated LTCC Front-end Module for IEEE 802.11a WLAN Applications

C.-H. Lee, S. Chakraborty*, A. Sutono**, S. Yoo, D. Heo*** and J. Laskar*

RF Solutions, Norcross GA 30071

*Yamacraw Design Center, School of ECE, Georgia Institute of Technology, Atlanta GA 30332

**Zepton Networks, Sunnyvale CA 94089

***National Semiconductor, Norcross GA 30071

***Abstract*** **— This paper presents the design, development and measurement of a highly-integrated and high linearity RF front-end module with integrated filter for IEEE 802.11a wireless LAN applications. The developed front-end MMIC includes LNA, PA, and SPDT switch integrated on a single chip in a commercial GaAs MESFET process. An embedded 3-D band pass filter has been integrated on the front-end module using LTCC technology. The performance of the front-end module is compliant to the HiPERLAN-I and IEEE 802.11a RF standards. The LNA exhibits 16.5 dB of gain, 2.1 dB of noise figure and IIP3 of 2.8dBm. The PA shows the 24 dBm output power and IM3 of better than 25dBc. The SPDT switch demonstrates 1.2 dB of insertion loss and 28dBm of input P1dB. To the best of our knowledge, this is the first report on C-band PA-LNA-Switch integrated on a single chip with embedded LTCC filter.**

## I. Introduction

Development of HiPERLAN-I [1] and IEEE 802.11a (HiPERLAN-II, upper U-NII) [2] standards has attracted a lot of interest in high data rate wireless transceivers in 5-6 GHz band. These standards incorporate Gaussian Minimum Shift Keying (GMSK) and Orthogonal Frequency Division Multiplexing (OFDM) as the modulation schemes, respectively. The OFDM signal exhibits a high peak to average power ratio and demands high linearity while the GMSK signal requires very small group delay variations in the RF front-end. It is desirable for the transceiver to be able to cover both the lower (5.15-5.35GHz) and upper (5.75GHz) UNII band. Earlier work in the 5-6 GHz band [3]–[5] barely meet the strict linearity requirements of the OFDM signal. Most of the single-chip front-end MMIC implementation has been focused on PCS-band applications [6]-[8].

This paper presents the development of a C-band front-end transceiver module that shows high linearity and broad band performance. Wide band performance of integrated circuits are very attractive due to their applicability for different applications as well as the potential for integration as multi-band wireless transceiver solutions. Fig. 1 shows the block diagram of the RF front-end module. These implemented MMIC and BPF are characterized and their measured performance is presented.

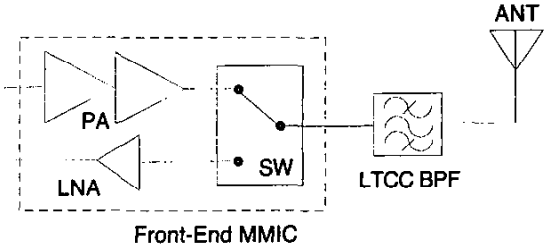


Fig. 1. Schematic diagram of RF front-end module.

## II. MMIC Design

The LNA, PA, and SPDT switch has been designed and integrated on a single chip. A photograph of the C-band RF front-end GaAs MMIC is shown in Fig. 2.

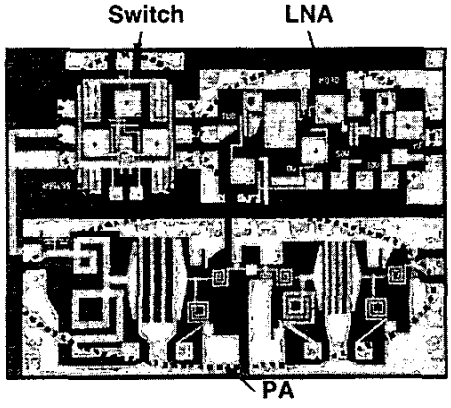


Fig. 2. Photograph of the RF front-end MMIC.



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The MMIC has been fabricated in Triquint Semiconductor Inc.'s TQTRx GaAs MESFET 0.6μm process and occupies less than 80×100 mils$^2$ die area.

### *A. LNA Design*

The LNA design utilizes a cascode topology with depletion mode GaAs MESFETs. A schematic view of the LNA is shown in Fig. 3. The optimum device gate width, 300 μm (6 finger 50 μm), is chosen to minimize noise figure in this cascode LNA [9]. High IIP3 and low DC power consumption are the two key features of the cascode LNA. The IIP3 is higher than that of the cascade design because the gain is high while distortion in the common gate stage can be minimized. The cascode LNA consumes half the power of a two-stage cascade LNA due to its current re-use. We utilize the depletion GaAs MESFET process since it exhibits better intermodulation distortion (IMD) performance than the enhancement MESFET. An inductive degeneration matching circuit is used for the input stage to achieve simultaneous noise and power gain as well as to improve stability. Both cascode LNA devices are biased with the same current, and the bias point is selected to achieve low noise figure, low dc power consumption, and moderate gain, simultaneously. Noise contribution of the gate biasing resistors is negligible. The output matching is optimized to achieve high gain and high IIP3.

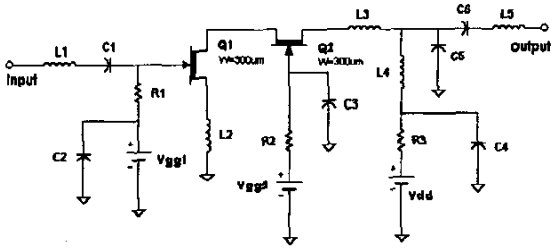


Fig. 3. Schematic diagram of cascoded LNA MMIC.

### *B. PA Design*

The IEEE802.11a transmitter requires a PA with high linearity and efficiency because of its high peak-to-average power ratio. The implemented PA has a two-stage single-ended configuration. The first and second stages employ 1.5 mm and 2.4 mm MESFET devices, respectively. The RF performance is optimized with reactive matching elements to achieve better linear operation. The inductors used in the circuit simulation were modeled as an equivalent circuit using S-parameters from EM simulation. The 40-μm width of metal was used for inductor on the drain side of second stage to overcome the current density limitation of the metal. To stabilize the PA at low frequencies, the shunt resistive stabilizing circuit on the gate side is incorporated as shown in Fig. 4.

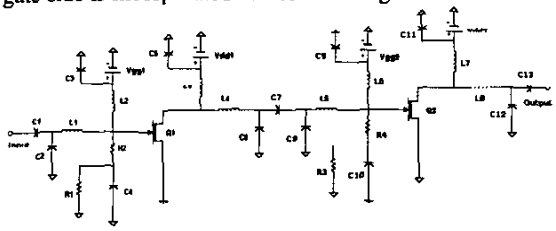

Fig. 4. Schematic diagram of 2-stage PA MMIC.

### *C. SPDT Switch Design*

RF Switch is widely used for antenna switching such as Tx/Rx and diversity. A switch has been designed in a single-pole double-throw (SPDT) configuration. For WLAN applications, there is a need for switch with compact size, higher power handling capability in lower voltage operation. To achieve the high P1dB with low voltage operation, D-FET with shallow pinch-off voltage (-0.6V) was selected [10]. The number of FET stacking was optimized for insertion loss and P1dB. It has a compact size of 30×30 mil$^2$. Fig. 5 shows the schematic diagram of the SPDT switch. The FET is acting as resistance with ON-state and capacitor with OFF-state. Choice of large device reduces the insertion loss due to its smaller ON resistance. However, beyond certain size, the parasitic capacitance of OFF-state is dominant to the ON-state resistance, resulting in the signal leakage. The optimum device size has been determined by a trade-off between the insertion loss and isolation considerations. The series FET has device size of 1.2mm and shunt FET has 0.6mm. The spiral inductor and MIM capacitor was fabricated for on-chip matching.

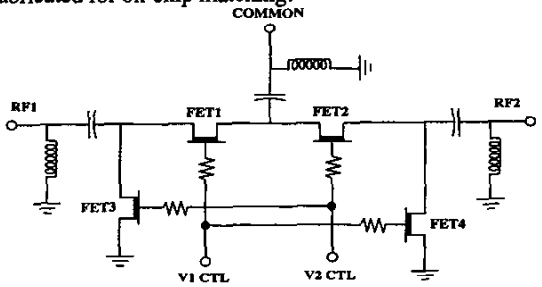


Fig. 5. Schematic diagram of SPDT switch MMIC.

## III. MMIC Measured Performance

The LNA exhibits a measured gain of 16.5 dB, noise figure of 2.1 dB, and IIP3 of 2.8 dBm at 5.8 GHz as shown in Fig. 6. The variation of noise figure is less than

0.4 dB over 5-6 GHz. Input and output return losses are 18 dB and 12 dB, respectively, at 5.8 GHz. The IIP3 performance was measured by applying two tones with equal power levels at 5.8 GHz and 5.7999 GHz. The measured +2.8 dBm of IIP3 was achieved, which meet the specification of an LNA for a 5.8 GHz OFDM wireless communication system. The LNA draws 13.2 mA with 3V dc supply and occupies die area of 50x20 mils$^2$.

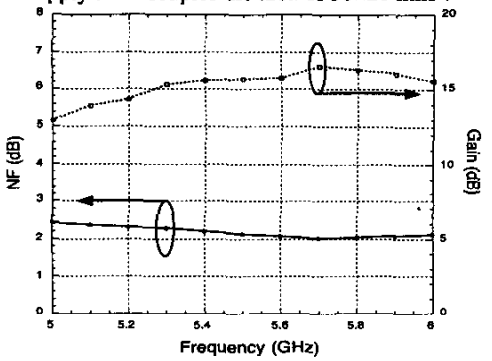


Fig. 6. Measured NF and gain of LNA.

TABLE I
SUMMARY OF MEASURED PA PERFORMANCE

| Specification | Measured Data |
|---|---|
| Operating Drain Bias | 5 V |
| Operating Frequency | 5.1 GHz ~5.8 GHz |
| Power Gain | 14~16 dB |
| Output P1dB | 24 dBm |
| OIP3 | 41 dBm |
| IM3 at P1dB | > 25 dBc |
| Harmonics at P1dB | > 28 dBc |
| Input VSWR | < 1.5 : 1 |

The measured performances of the PA are shown in TABLE I. The output P1dB and output IP3 (OIP3) is 24 dBm and +41 dBm, respectively, at 5.8 GHz. The IMD3 at P1dB point is larger than 25 dBc with 5MHz offset frequency. The size of the PA MMIC is 100x40 mils$^2$.

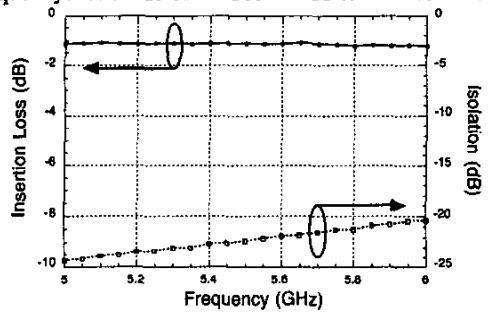


Fig. 7. Measured insertion loss and isolation of SPDT switch.

The SPDT switch demonstrated a measured insertion loss of 1.2 dB and isolation of better than 20 dB from 5 to 6 GHz in 4/0 V operation as shown in Fig. 7. The switch shows the measured output P1dB of 28 dBm in 4 V operation at 5.8 GHz. Each port has better than 13 dB of return loss through the operating frequency band due to on-chip matching.

The LNA combined with switch exhibits a measured gain of 15 dB, a noise figure of 3.5 dB, and an IIP3 of 4.4 dBm at 5.8 GHz as shown in Fig. 8.

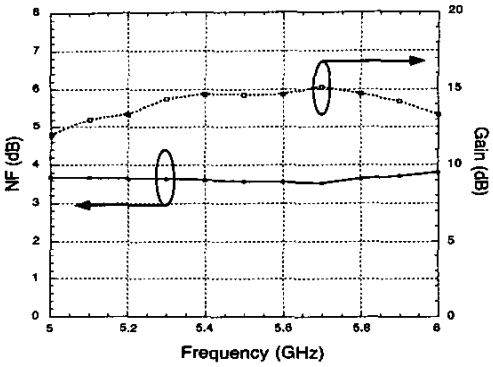


Fig. 8. Measured NF and gain of LNA combined with switch.

## IV. MODULE DESIGN AND MEASURED PERFORMANCE

Fig. 9 shows the exploded view of embedded stripline bandpass filter designed in a folded coupled stripline configuration using LTCC process. The filter, built using Dupont 943AT tapes, is embedded between the front-end MMIC and the antenna to reject the spurious signals.

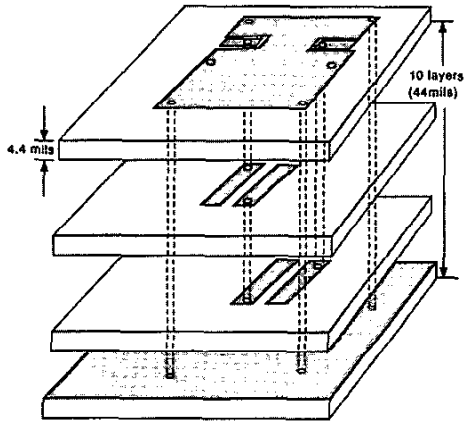


Fig. 9. Exploded view of embedded LTCC filter

Measured performance of the prototype filter indicates a 3.5 dB of insertion loss and 15 dB of return loss at 5.8 GHz, as well as less than 200 MHz bandwidth, as shown

in Fig. 10, to allow a good rejection (23dB) at the image frequency of 4.8 GHz. This on-package LTCC filter demonstrates comparable performance to the C-band MCM-D filter reported in [11]. The entire receiver chain exhibits a total gain of 11.5 dB incorporating the filter and wirebond loss at 5.8 GHz as shown in Fig. 11. Fig. 12 shows the photograph of the implemented LTCC-based RF front-end module with integrated filter. The module requires 10 tape layers and the total size is 8x9x1.1 $mm^3$.

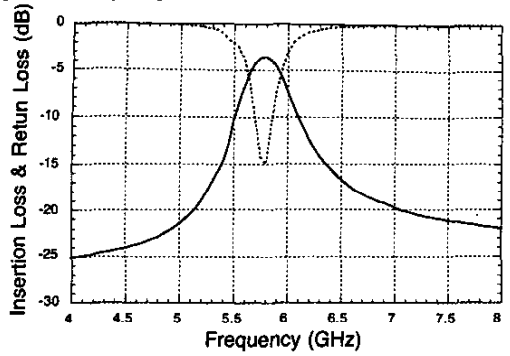


Fig. 10. Measured insertion loss and return loss of LTCC filter.

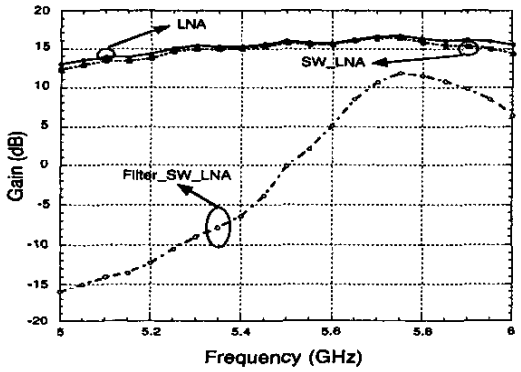


Fig. 11. Measured gain performance of entire receiver chain.

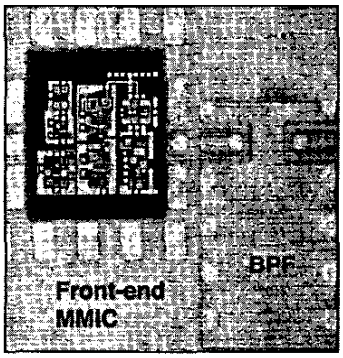


Fig. 12. Photograph of the Implemented LTCC-based front-end module with integrated band pass filter.

## V. Conclusion

We have reported the development of a highly integrated, broad band, and high linearity GaAs transceiver front-end module with integrated LTCC filter compliant with the 5-6 GHz wireless communication band standards, HiPERLAN-I and IEEE 802.11a. The performance of the developed MMIC and module show significant linearity improvement over earlier reported implementations while maintaining broad band characteristics. To the best of our knowledge, this is the first report on PA-LNA-Switch integrated on a single chip with embedded LTCC filter.

## Acknowledgement

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